## AMENDEMENTS TO THE SPECIFICATION

Please replace paragraph [0033] of the Specification with the following amended paragraph:

**[0033]** As the buffer 126 acts as a cache memory, its size and/or manner of operation can be tailored to the access usage of the NAND architecture Flash memory device 100 by the host 102. This allows for an as efficient data access as possible given the expected data usage of the memory device 100. For example, the memory device 100 can be tailored for small data/block accesses, sequential data accesses, large data/block access, and so on. For random reads and/or writes, caching data management/replacement methods, including, but not limited to, translation look aside buffers, least recently used (LRU) data word replacement, and write-through caching, can also be used to great effect. In one embodiment of the present invention, a optional special purpose "ready/busy" external connection pin 134 or internal status register/flag 132 of the NAND architecture Flash memory device 100 may be monitored to indicate the status of the memory. This allows the memory device 100 to signal that it is busy with a read or write access (due to read or write latency, etc.), and causes the host 102 to wait, halting data transfers when active or set.